

2nd Generation QUATARA Flight Computer

Completed Technology Project (2014 - 2015)

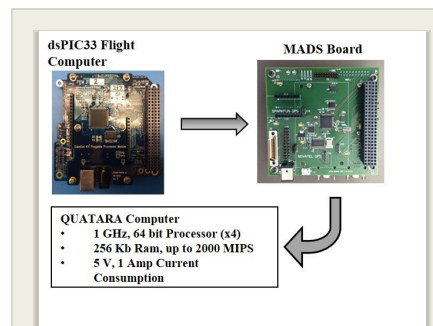


Project Introduction

The primary objective of this activity is to develop, design, and test (DD&T) the QUAD-core siTARA (QUATARA) computer to distribute computationally intensive processes such as: communication, sensors, attitude determination, attitude control, cameras, robotic manipulators, and science payloads. An example of the current state-of-the-art for a COTS CubeSat flight computer is, a 16 bit 80 MHz Microchip dsPIC33 microcontroller capable of managing the satellite attitude determination, control system, communication system, power, and science payloads. Adding more capability to these COTS flight computers required the development, under a previous CIF proposal, of the Modular Attitude Determination System (MADS) board. MADS lessened the I/O load from the flight computer so it could focus on higher priority tasks such as managing a Real-Time Operating System (RTOS) or carrying out an attitude control algorithm. The MADS board utilized a 16 bit 80 MHz Texas Instruments ARM Cortex-M4 Stellaris microcontroller to execute the attitude determination algorithm independently of the dsPIC33 flight computer. Once the MADS board processes the data, the dsPIC33 receives the estimated states and determines the desired attitude control.

The addition of cameras, proximity sensors, robotic manipulators, thruster systems, complex science payloads and video guidance systems, would cause current CubeSat flight computers to be overwhelmed. Because of the desire to expand the capabilities of CubeSats, the innovation of the QUATARA architecture enhances the capabilities of data handling and computer processing by replacing the 16 bit 80 MHz microcontrollers with four 64 bit 1 GHz microprocessors. The QUATARA allows for tasks to be processed at a faster rate not only because of the difference in clock speed between the platforms but also because of the fact that there are four individual microprocessors which can run these tasks independently without the need to serialize the execution of the code like in a single microcontroller.

The QUATARA computer aims to be fault-tolerant by means of a software voting scheme to guard against the effects of Single Event Effects (SEE) such as Single Event Upsets (SEU). Each 'node' (Gumstix Computer-On-Modules (COM)) of the QUATARA computer will be connected to its own set of sensors and actuators. These individual nodes will collect their respective data and share it between themselves over a data bus (such as RS-485). Once each node has all the data from all of the other nodes it will process it and come up with a result. This result can then be used to determine if a node is considered as 'failed' and that node then needs to be disabled, (this can be done by ignoring future data received from that node or by completely shutting it off). In the case a node is lost a support node is available to be switched in for the failed node. This support node will focus on low priority tasks, (such as housekeeping), if it is not required as a voting node. Synchronization between the nodes can be maintained by having a precise timing source on each of the processors, (such as a ticking timer interrupt routine), that ticks at a set time interval. This timing information will be passed between the nodes and the tick



Top-level schematic for Flight Computer Systems Development

Table of Contents

Project Introduction	1
Anticipated Benefits	2
Primary U.S. Work Locations and Key Partners	2
Organizational Responsibility	2
Project Management	2
Images	3
Project Website:	3
Technology Maturity (TRL)	3
Technology Areas	3

2nd Generation QUATARA Flight Computer

Completed Technology Project (2014 - 2015)

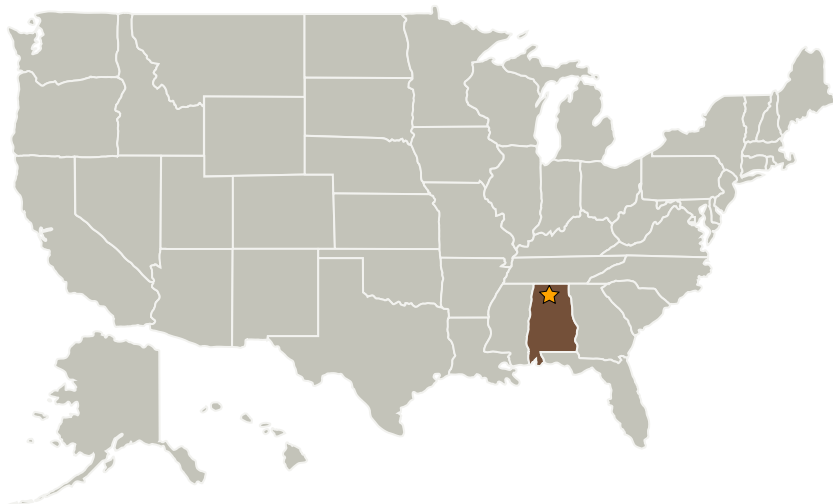


rate of the interrupt routine will be modified as required to ensure that all of the nodes data remains in sync.

Anticipated Benefits

Developing the fault tolerant capability of the 2nd Generation QUATARA enables new missions such as Sample Return, Debris Removal, Satellite Inspection, Peer to Peer Refueling, and Formation Flying which are not currently possible due to the lack of CubeSat flight computers with a sufficiently high level of fault tolerance that would be required for these types of missions.

Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★ Marshall Space Flight Center (MSFC)	Lead Organization	NASA Center	Huntsville, Alabama

Primary U.S. Work Locations

Alabama

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Center / Facility:

Marshall Space Flight Center (MSFC)

Responsible Program:

Center Innovation Fund: MSFC CIF

Project Management

Program Director:

Michael R Lapointe

Program Manager:

John W Dankanich

Project Manager:

Andrew Keys

Principal Investigator:

Jose Molina Fraticelli

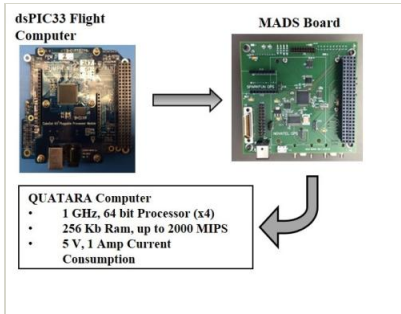
Co-Investigators:Steven R Peeples
Pedro A Capo-lugo

2nd Generation QUATARA Flight Computer

Completed Technology Project (2014 - 2015)



Images



Molina 1

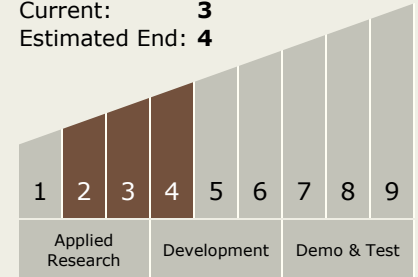
Top-level schematic for Flight Computer Systems Development
(<https://techport.nasa.gov/image/13345>)

Project Website:

<https://www.nasa.gov/directorates/spacetech/home/index.html>

Technology Maturity (TRL)

Start: **2**
Current: **3**
Estimated End: **4**



Technology Areas

Primary:

- TX11 Software, Modeling, Simulation, and Information Processing
 - └ TX11.6 Ground Computing
 - └ TX11.6.4 Quantum Computer